1.5×10^{-9} Ω·cm^2 Contact Resistivity on Highly Doped Si:P Using Ge Pre-amorphization and Ti Silicidation

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Abstract

Record-low contact resistivity (ρ_c) for n-Si, down to 1.5×10^{-9} Ω·cm^2, is achieved on Si:P epitaxial layer. We confirm that Ti silicidation reduces the ρ_c for n-Si, while an additional Ge pre-amorphization implantation (PAI) before Ti silicidation further extends the ρ_c reduction. *In situ* doped Si:P with P concentration of 2×10^{21} cm^{-3} is used as the substrate, and dynamic surface anneal (DSA) boosts P activation. In addition, TiO_x based metal-insulator-semiconductor (MIS) contact is also studied on Si:P but is found to suffer from low thermal stability.

1. Introduction

The external resistance of transistors is much determined by the metal-semiconductor contact resistivity (ρ_c) and the semiconductor bulk resistivity (ρ_b). *In situ* doped low-ρ_b Si:P epitaxial layer has been demonstrated [1,2], and sub-1×10^{-8} Ω·cm^2 ρ_c have also been reported on Si:P [3,4]. These previous studies feature heavy P incorporation and high P activation. In this work, ultralow ρ_c are further explored on Si:P by i) dynamic surface anneal (DSA) [5], ii) Ge pre-amorphization + Ti silicidation (PAI+$TiSi_x$) [6-8], and iii) TiO_x based metal-insulator-semiconductor (MIS) contact [9-11]. Combining the first two solutions, record-low ρ_c of 1.5×10^{-9} Ω·cm^2 is achieved on heavily doped Si:P, which meets the ρ_c requirement for the N7 node and beyond [12]. This sub-1×10^{-8} Ω·cm^2 ρ_c study was carried out with a novel high-accuracy multiring circular transmission line model (MR-CTLM) [3].

2. Experimental

For MR-CTLM (Fig.1), Si:P with two P concentrations (N_d), 3×10^{20} cm^{-3} P (Si:P-3E20) and 2×10^{21} cm^{-3} P (Si:P-2E21), were grown in an ASM Intrepid^{TM} XP epi reactor. 8keV 3×10^{15}cm^{-2} P ion implanted (P I/I) Si wafers, activated by a 1000°C spike anneal, were compared with epitaxial Si:P. A 2-pulse 1200°C 0.25 ms DSA was applied to further activate P. 5 nm Ti was used as the contact metal. Two modules—PAI+$TiSi_x$ and MIS—are specified in Table I and Table II, respectively. For the $TiSi_x$ and MIS experiments, Schottky barrier diodes (SBD) were prepared on lightly doped n-Si wafers.

Four-fin transmission line devices (4Fin-TLM) were also fabricated (Fig. 2) to study the compatibility of Si:P with 3-D fin structure. Si:P-2E21 was epitaxially grown on top of fins after a Si recess. Next to that, DSA was applied and followed by the rest of standard metallization processing.

3. Si:P with DSA

For both Si:P-3E20 and Si:P-2E21, DSA boosts the P activation and thus reduces Si:P sheet resistance (R_s) and ρ_c (Fig.4a). In a previous study [1], we found that, after 1200°C DSA, almost all P is activated in Si:P-3E20, and around 9×10^{20} cm^{-3} P is activated in Si:P-2E21. Clearly, Si:P has several advantages over I/I n^+Si. Si:P, combined with DSA, has a much higher P activation efficiency than P I/I n^+Si; while P I/I n^+Si is insensitive to DSA (Fig.4a), even though a large amount of inactivated P is still seen at the Si surface (Fig.4b). Moreover, compared with the P profile by I/I (Fig.4b), Si:P has a much better controlled box-shaped profile [1,2]. Further, when used for source/drain in multi-gate devices, Si:P avoids I/I induced damage. On both planar (Fig.5) and fin structures (Fig.6b), XTEM shows high-quality Si:P after processing. The DSA also improves R_c on 4Fin-TLM (Fig.7).

4. Si:P with PAI+TiSix

The ρ_c studies in this section are all performed on DSA enhanced Si:P. In has been found that silicidation at 400-600°C reduces ρ_c for Ti, Zr, Hf, and V/n-Si [14,15]. In this work, we use a pre-amorphization technique to enhance the Ti silicidation and further reduce ρ_c. Previous studies on Ge PAI+$TiSi_x$ have shown the following advantages: i) Si diffusion during $TiSi_x$ growth leads to a vacancy injection into Si substrate, while Ge PAI creates end-of-range (EOR) interstitial defects. These two types of defects can recombine with each other [6]. ii) The thermal budget required for $TiSi_x$ growth is lowered by PAI [7,8]; iii) high P concentration normally suppresses the silicidation process, while PAI releases this suppression [8].

In this work, shallow PAI (Table I) and moderate silicidation temperatures are studied to seek compatible solutions for downscaled multi-gate devices. During an anneal of samples with PAI+$TiSi_x$, two processes occur simultaneously—Ti silicidation and amorphized Si solid phase epitaxial regrowth (SPER). Fig.8 shows PAI1 particularly boosts the silicidation. PAI1 has a higher Ge dose/depth ratio than PAI2 and PAI3. Grazing incidence XRD (GIXRD) (Fig.9) confirms $TiSi_x$ occurs at a lower temperature in the case of PAI1 than NoPAI, which is consistent with [7,8]. The ρ_c (Fig.10) and the XTEM (Fig.11) show the SPER of PAI1 is completed at 550°C. Note that EOR defects (Fig.11a) disappear after 550°C RTP (Fig.11b) due to the defect recombination [6].

After 550°C RTP, PAI1 and PAI2—different dose but with same low energy—show promising ρ_c (Fig.12). Note that

NoPAI also improves with 550°C RTP (Fig.12). A detailed RTP study of NoPAI and PAI1 on Si:P-3E20 (Fig.13) and SBD (Fig.14) shows the low ρ_c at 500-550°C is accompanied by low-φ_b $TiSi_x$ formation. The observed ρ_c and φ_b variation trends for NoPAI are consistent with previous studies [14,15]. PAI1 outperforms NoPAI due to the aforementioned defect recombination [6] and improved silicidation [7,8]. Interestingly, on Si:P-2E21 (Fig.15), NoPAI is insensitive to RTP below 550°C, possibly because the large amount of P in Si:P-2E21 retards silicidation [8,14]. But for PAI1, the minimal ρ_c, 1.5×10^{-9} $\Omega\cdot cm^2$, is still reached at 525°C due to PAI enhanced Si diffusion and silicidation [7,8].

5. Si:P with MIS

The TiO_x based MIS contact scheme is known to reduce the Schottky barrier height by relieving the Si surface pinning [10,11]. In this work, several TiO_x based MIS contact schemes (Table II) are compared on Si:P. But after a processing with moderate post-metal thermal budget (370-400°C for several min), we find negligible difference in ρ_c and φ_b between MS and MIS (Fig.16). XTEM (Fig.17) shows the oxide is missing in the MIS sample, and XPS (Fig. 18) detects that O diffuses into Ti.

In contrast, by limiting post-metal processing temperature below 250°C, clear difference between as deposited MIS and MS is seen: MIS3 has a lower φ_b but a higher ρ_c (Fig.19). This indicates that the 1 nm amorphous ALD TiO_2 in MIS3 has a high conduction band offset with Si [17] and thus a high tunneling resistance. With a follow-up RTP study, ρ_c of MIS3 decreases a lot (Fig19c) [10], which is, however, not attributed to low φ_b: φ_b gets higher than 0.3 eV after an RTP at 300-500°C (Fig.19ab); simulation and XTEM (Fig.20) disclose that, due to O diffusion, MIS3 already becomes MS-like contact and thus has close properties to the MS control.

Though the MIS thermal stability has seldom been discussed systematically in literature yet, we speculate that the low thermal stability is a universal problem for all MIS contact schemes. Because n-type semiconductor oriented MIS contact scheme requires a low work function metal (LWFM): LWFM, such as Ti, Al, and Mg, are typically reactive. Therefore, it will be difficult to prevent all the reaction and interdiffusion between LWFM and an ultrathin insulator in MIS. This low thermal stability limits the chances for MIS to survive the thermal budget during back-end processing.

6. Benchmarking and Conclusions

DSA enhanced P activation in heavily doped Si:P benefits sub-1×10^{-8} $\Omega\cdot cm^2$ ρ_c explorations (Fig. 21). We introduce a Ge PAI+$TiSi_x$ technique on Si:P with P of 2×10^{21} cm^{-3}, and achieve a record-low ρ_c of 1.5×10^{-9} $\Omega\cdot cm^2$. This low ρ_c meets the ρ_c requirement for the N7 node and beyond. In addition, we discuss the thermal stability of MIS contacts. The low thermal stability may limit the application of MIS into realistic manufacturing.

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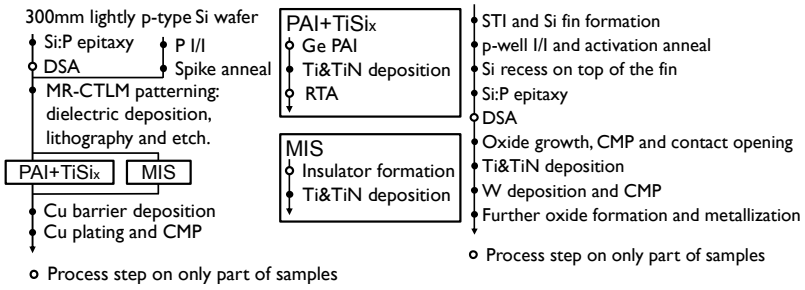


Fig. 1 Process flow of MR-CTLM shown at left side. Modules of PAI+TiSi$_x$ and MIS are specified at right side, respectively. The detailed module conditions are described in Table I and Table II.

Fig. 2 Process flow of 4Fin-TLM. Fins were fabricated with self-aligned double patterning (SADP).

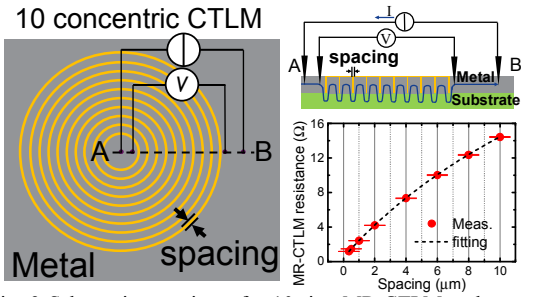


Fig. 3 Schematic top view of a 10-ring MR-CTLM and cross sectional view along dashed line AB. A typical MR-CTLM fitting is shown based on 9 sets of measurement points. Small error bars (standard deviations) reflect high precision and reproducibility of process, measurement and ρ_c extraction [3].

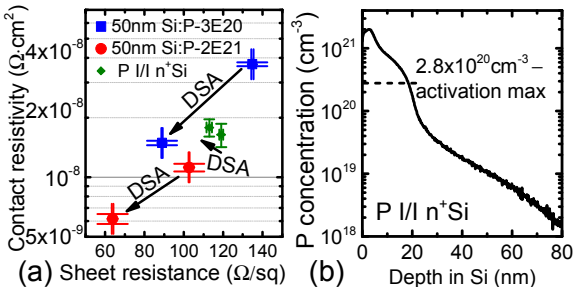


Fig. 4 a) Impact of DSA on ρ_c and R_s for Si:P-3E20, Si:P-2E21 and P I/I n^+-Si, respectively. Ti is the contact metal. P profile in I/I n^+-Si is shown in b). The activation maximum in b) is calculated based on Rs and the empirical resistivity-P concentration relation in [13].

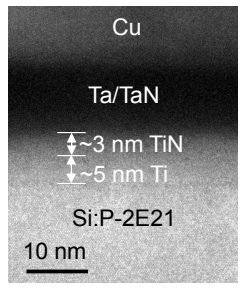


Fig. 5 XTEM of Ti/Si:P-2E21 contact. No defects are seen in the Si:P layer and the surface is smooth.

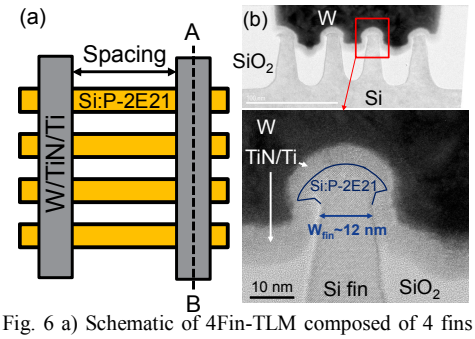


Fig. 6 a) Schematic of 4Fin-TLM composed of 4 fins in parallel. XTEM along dashed line AB is shown in b). W_{fin} is ~12 nm. Fins in b) received 1200°C DSA and remain high quality. Boundary between Si:P and Si fin is invisible due to good epitaxial quality.

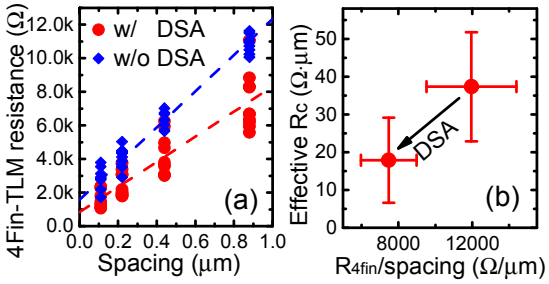


Fig. 7 a) 4Fin-TLM resistance vs spacing, and b) extracted R_c of Ti/Si:P-2E21 on fins. DSA reduces R_c. Dash line in a) illustrates the curve fitting, which gives an intercept at zero spacing. Effective R_c is calculated by (intercept/2)×4W_{fin}.

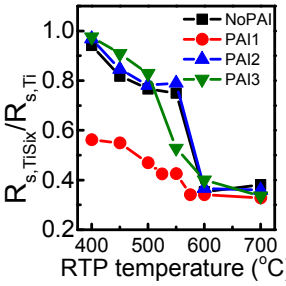


Fig. 8 R_s of TiSi$_x$ vs RTP temperature. In ordinate axis, R_s of TiSi$_x$ is divided by Rs of as deposited Ti. RTP was performed in N_2 for 1 min.

Table I Ge PAI conditions and induced amorphized Si thicknesses prior to Ti/TiN deposition. The NoPAI sample serves as control.

ID	PAI Energy	Ge dose	a-Si thickness*
NoPAI	w/o PAI	0	0
PAI1	3 keV	6×10^{14} cm^2	6.0 nm
PAI2	3 keV	3×10^{14} cm^2	3.7 nm
PAI3	10 keV	6×10^{14} cm^2	18.6 nm

*Measured by Rutherford backscattering spectrometry (RBS)

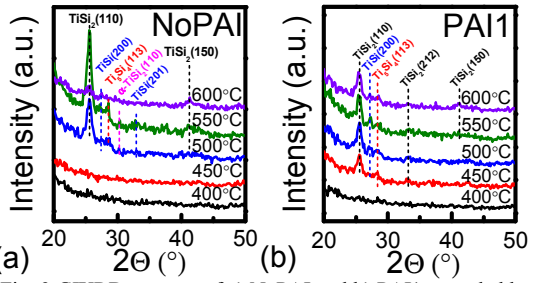


Fig. 9 GIXRD patterns of a) NoPAI and b) PAI1 annealed by 1 min in N_2 over temperature range of 400-600°C. Ti silicidation of PAI1 starts at 450°C, while that of NoPAI starts at 500 °C. Mixture of several TiSi$_x$ phases is seen at 500-550°C for both samples.

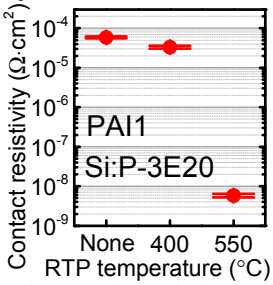


Fig. 10 ρ_c of PAI1 before and after RTP at 400 and 550°C. The high ρ_c after 400°C RTP implies there is insufficient SPER.

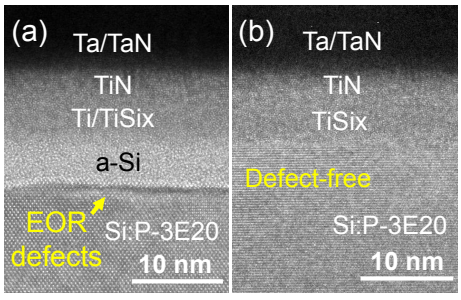


Fig. 11 XTEM of PAI1 after a) 400°C and b) 550°C RTP. For 400°C RTP, a-Si is not fully recrystallized; EOR defects caused by the Ge PAI are seen. For 550°C RTP, SPER is completed and EOR defects are eliminated. EDS analysis (not shown) of b) shows Ti:Si equal to 46%:54% in the TiSi$_x$ layer.

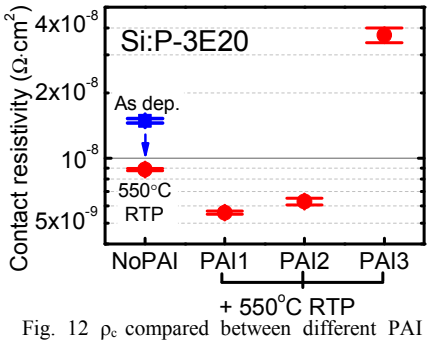


Fig. 12 ρ_c compared between different PAI conditions after 550°C RTP. The as deposited NoPAI serves as a control. NoPAI also improves after 550°C RTP.

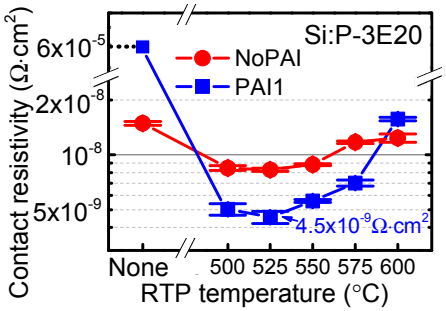


Fig. 13 ρ_c of NoPAI and PAI1 after 500-600°C RTP. Compared with as deposited Ti/Si:P-3E20 contact, 525°C RTP reduces ρ_c by 1.8 times, while PAI1 + 525°C RTP reduces ρ_c by 3.2 times.

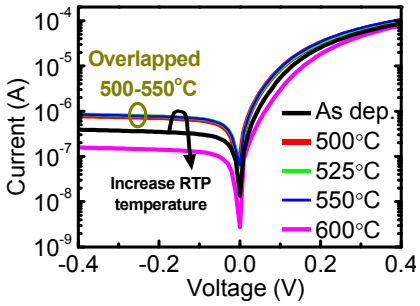


Fig. 14 Current-voltage curves of NoPAI SBD before and after RTP. φ_b decreases at 500-550°C, and increases at 600°C.

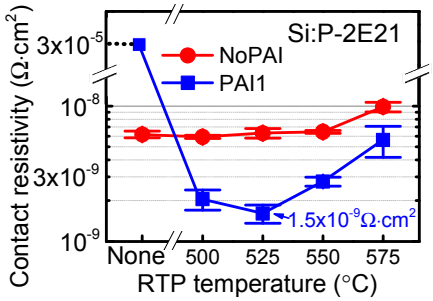


Fig. 15 ρ_c of NoPAI and PAI1 after 500-575°C RTP on Si:P-2E21. Record-low ρ_c for n-Si achieved by Si:P-2E21+DSA+ PAI1+525°C RTP.

Table II Insulator formation conditions for the MIS experiment. The MS contact serves as control.

ID	Before Ti&TiN deposition
MS	Bare Si
MIS1	~1.0 nm chemical SiO_x on Si
MIS2	0.5 nm ALD TiO2 on Si
MIS3	1.0 nm ALD TiO2 on Si

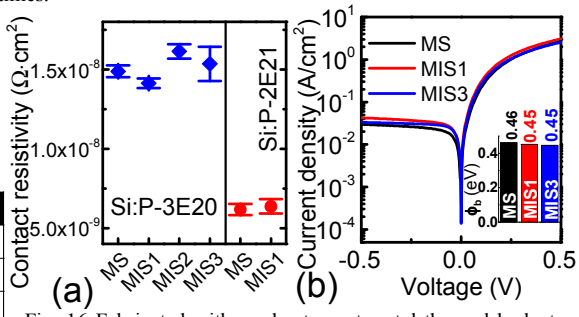


Fig. 16 Fabricated with moderate post-metal thermal budget, a) ρ_c and b) SBD properties show little difference between MS and MIS samples.

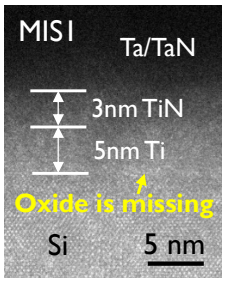


Fig. 17 XTEM shows no oxide in MIS1 after processing with moderate post-metal thermal budget.

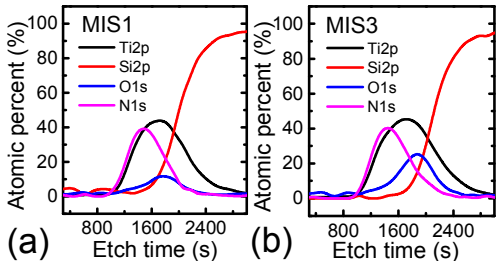
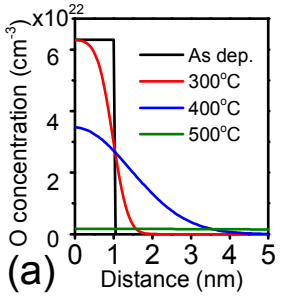


Fig. 18 XPS shows O signal is throughout Ti for a) MIS1 and b) MIS3, both fabricated with moderate post-metal thermal budget.



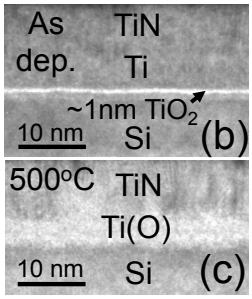


Fig. 20 a) Simulated O profile in MIS3 after 1 min RTP using O diffusion coefficient in Ti [18] and TiN [19], respectively. XTEM of MIS3, fabricated with low post-metal thermal budget, b) before and c) after 500°C suggests O diffusion from TiO_2 into Ti, consistent with simulation in a).

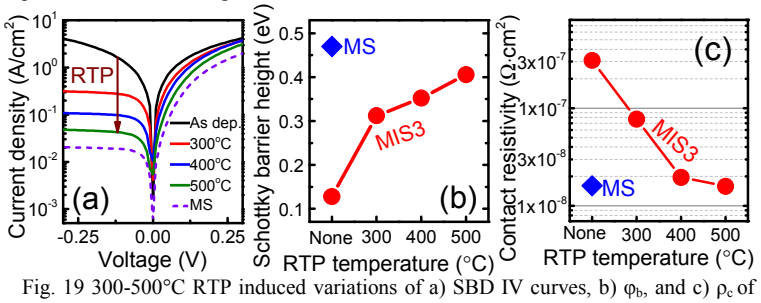


Fig. 19 300-500°C RTP induced variations of a) SBD IV curves, b) φ_b, and c) ρ_c of MIS3 samples, which were fabricated with low post-metal thermal budget. φ_b increases due to loss of TiO_2 based depinning or repinning. ρ_c decreases due to reduction of the insulating TiO_2. The low φ_b in b) are derived by cryogenic capacitance-voltage measurement. Samples in c) were fabricated on P I/I n^+-Si, whose doping condition was shown in Fig. 4b.

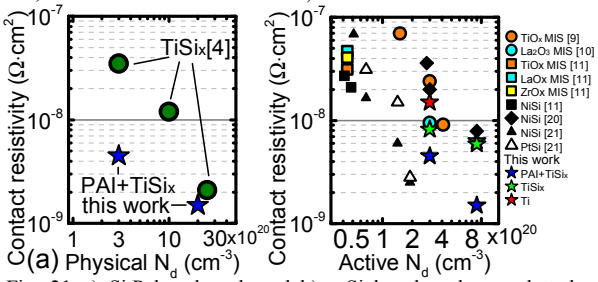


Fig. 21 a) Si:P benchmark and b) n-Si benchmark are plotted separately because active N_d is not provided in [4].